SRI International

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Covering the Period 1 January through 31 January 2010

POWER MEMS DEVELOPMENT

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Submitted in accordance with Deliverable A001 - Monthly Technical and Financial
SRI Project P19063

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ACTIVITIES AND PROGRESS

MEMS RESETTABLE CIRCUIT BREAKER (TASK 1.1) AND MEMS SWITCH FOR DC-DC VOLTAGE CONVERTERS (TASK 1.2)

Task 1.1 Contributors: Susana Stillwell, Sunny Kedia, Weidong Wang

Task 1.1 Deliverable: 10 prototype packed MEMS-based resettable circuit breakers for testing and analysis in ONR laboratories.

Task 1.2 Contributors: Sunny Kedia, Shinzo Onishi, Scott Samson

Task 1.2 Deliverable: Functional MEMS-based DC-DC converter in a vacuum package.

Task 1.1 and Task 1.2 Progress:

Full Wafer Fabrication (Rev A)

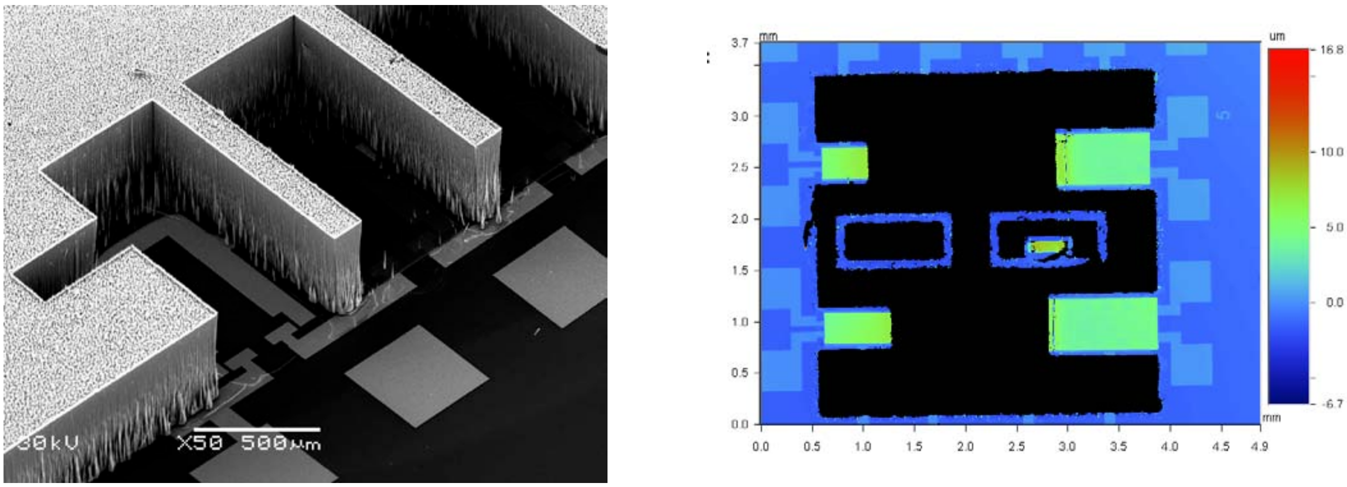
The resettable circuit breaker cantilevers use silicon dioxide (SiO_2) for temperature compensation. The compressive stress in the SiO_2 causes the cantilever to bow upwards 400 µm after release. In the DC-DC voltage converter the gap between the electrodes is 1.4 µm. After release, the cantilevers are stuck down. We devised a short loop experiment to better understand the cantilever behavior by omitting the contact metal and SiO_2 layers from test cantilevers.

Si Only Cantilever Short Loop

We developed an experimental plan to fabricate silicon-only cantilevers with the existing rev1.0 mask set. We patterned the silicon-on-insulator (SOI) wafer (cantilever wafer) with the release and the metal3 (bond metal) masks. The release mask defines the handle silicon area that is etched to allow the cantilever to move. The metal3 layer defines the bonding area to a double-sided polished (DSP wafer). We patterned the DSP wafer, or substrate wafer, with the indent (3.1 µm deep) and metal1 (bond metal). We bonded the SOI and DSP wafers together using Au-Au thermal compression bonding at 360ºC with a force of 800N for 45 min. Following the bonding, we etched the handle silicon using deep reactive ion etching (DRIE). To release the cantilevers, we etched the buried oxide on the SOI wafer using reactive ion etch (RIE). Figure 1 shows a SEM image and an optical profilometer image of MEMS resettable circuit breaker. Figure 2 shows a SEM image and an optical profilometer image of the MEMS switch for DC-DC voltage converter. The smaller cantilevers (<1000 µm) have a slight downward bow that we hypothesize is due to thermal effects and permanent deformation of the metals during bonding or a thermal and charging effect from the reactive ion etch. The larger cantilevers bow enough to cause contact with the bottom electrode. The optical profilometer data suggest that the smaller cantilevers have an acceptable gap of 2-3 µm between the cantilever and the bottom electrode. Using these data we developed a Rev B full wafer fabrication process.

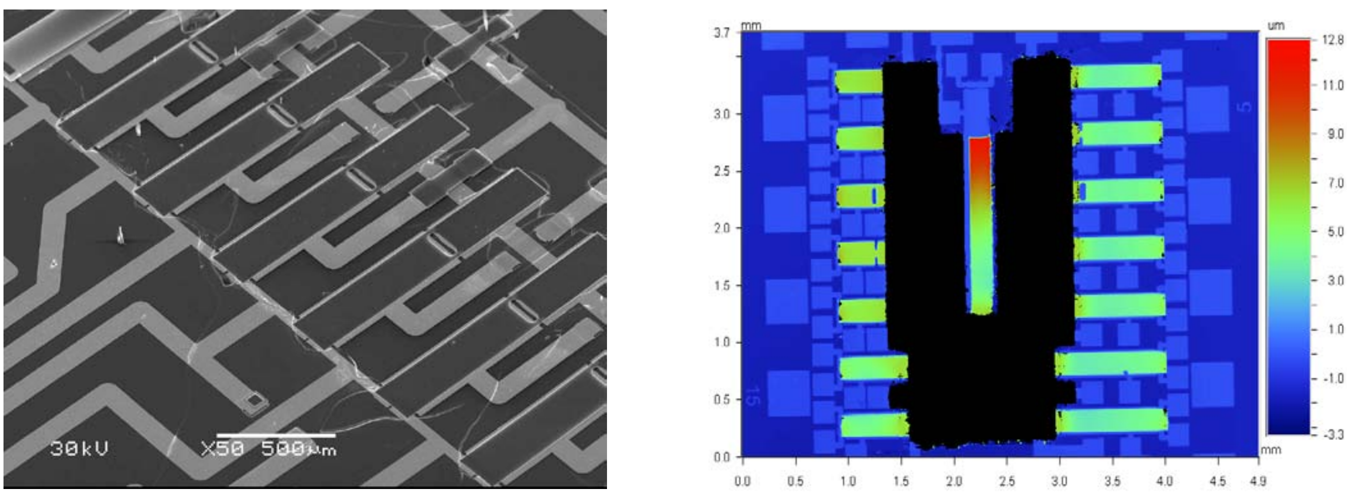
Full Wafer Fabrication (Rev B)

For the Rev B process, the indent is increased by 2 µm to 5 µm. For the resettable circuit breaker, tensile deposited silicon nitride is used for thermal compensation in place of compressive thermally grown SiO_2. The tensile stress of the silicon nitride film causes the cantilever to bow downward or come in contact with the bottom electrode, closing the circuit for the MEMS circuit breaker. For the DC-DC voltage converter, thinner (200 nm) SiO_2 is used as contact isolation material at each cantilever tip. This balances the tensile stress from metal with compressive stress from oxide, keeping the cantilever from touching the bottom electrode. The fabrication of Rev B wafers is currently in progress.



(a) (b)

Figure 1: a. SEM image of the resettable silicon-only cantilevers after release; b. optical profilometer image of chip style E7 illustrating reduced bow of the cantilevers.



(a) (b)

Figure 2: a. SEM image of the DC-DC voltage converter after release; b. optical profilometer image of chip style D9 illustrating acceptably flat cantilevers on shorter cantilevers.

DIAMOND HEAT SPREADER OR HEAT SINK FOR HIGH POWER MEMS SWITCHES APPLICATIONS (TASK 1.3)

Contributors: Priscila Spagnol, Shinzo Onishi, Drew Hanser, John Bumgarner

Deliverable: Prototype device fabricated on a thin-film diamond heat spreader layer and individual samples of diamond on Si or other suitable substrates for material evaluation.

Progress:

Thermal conductivity measurement using 3 ω method. We identified and evaluated several experimental issues with our previous measurement setup and addressed several of these this month:

- To simplify measurements and to acquire better quality (improved repeatability, lower noise) data, we designed a robust new heater/sensor wire. The measurement terminals can be connected using a probe station, a four-point probe, or silver paint, which provides more flexibility.
- New wire patterns provide accurate measurement by eliminating the end effects.

The thermal conductivities (κ_S) of the diamond film calculated from the measurements made at the different frequency ranges shown in Figure 3 (b) and (d) were 920 and 1030 [$W{\cdot}K^{-1}{\cdot}m^{-1}$], respectively. We believe the difference between both measurements is due to resistive end effects in the bridge circuit, which we will work to address next month with circuit modifications. We continue to deposit thick crystalline diamond films, which will be used as a heat sink for the MEMS resettable circuit breaker. Additionally, a computer-based control system is being set up to automate data collection from the measurement circuit.

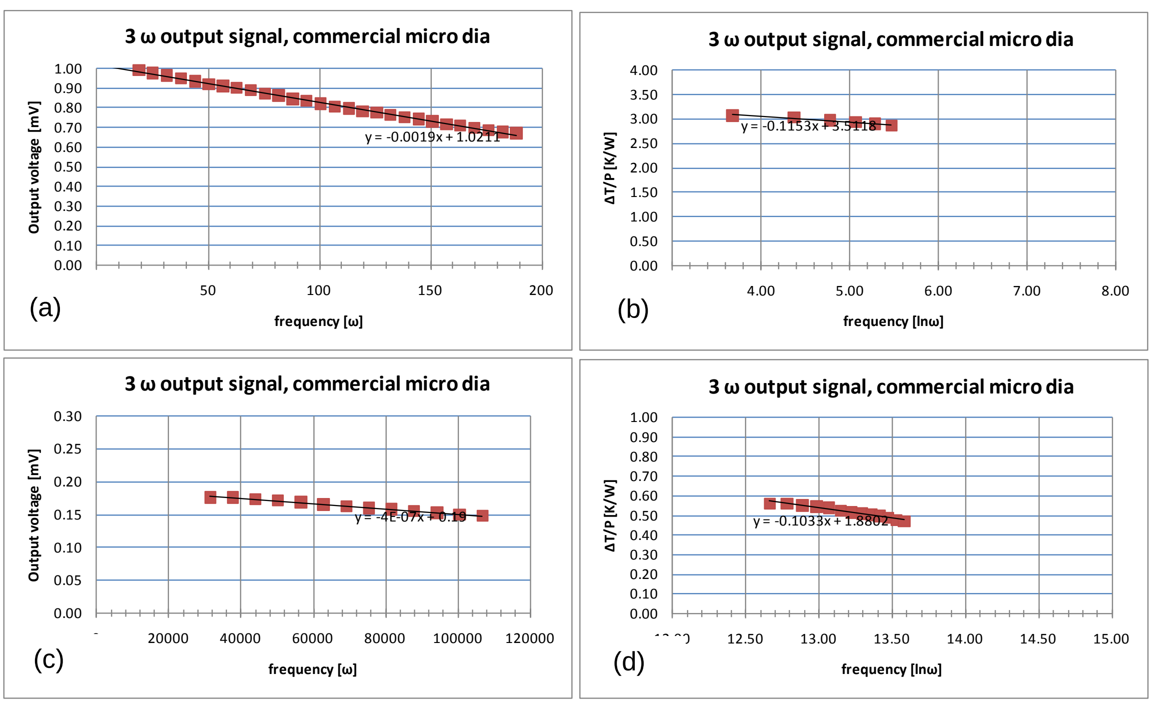


Figure 3: Measurements on a commercial microcrystalline diamond film (15-µm-thick, polished): (a) output voltage vs. omega frequency at low frequency; and (b) ΔT/P x log frequency, also at low frequency; (c) same plot as (a) but at higher frequency; (d) same plot as (b) but at higher frequency.

POSITRON TRAPPING AND STORAGE (TASK 2)

Contributors: Ashish Chaudhary, Friso van Amerom, Tim Short

Deliverable: A minimum of four MEMS-based trap structures for RF trapping of electrons

Progress:

Fabrication

We identified critical process issues in the first two fabrication runs and resolved them in the subsequent two process optimization iterations. The first electron trap (ET) prototype was completed and is ready for initial testing. The surface resistance of the atomic layer deposition (ALD) ZnO was measured to be about 20 times higher than expected. This is believed to be caused by a lower than expected deposition temperature at the top surface, due to a thermal gradient across the substrate. Despite the higher surface resistance, the SEM analysis of the surface showed good charge dissipation, and we do not anticipate surface charging during testing. In the future, the ALD ZnO deposition recipe can be modified to achieve a lower resistivity, if needed. Figure 4 shows the surface electrodes and bond pads at the end of the ET.

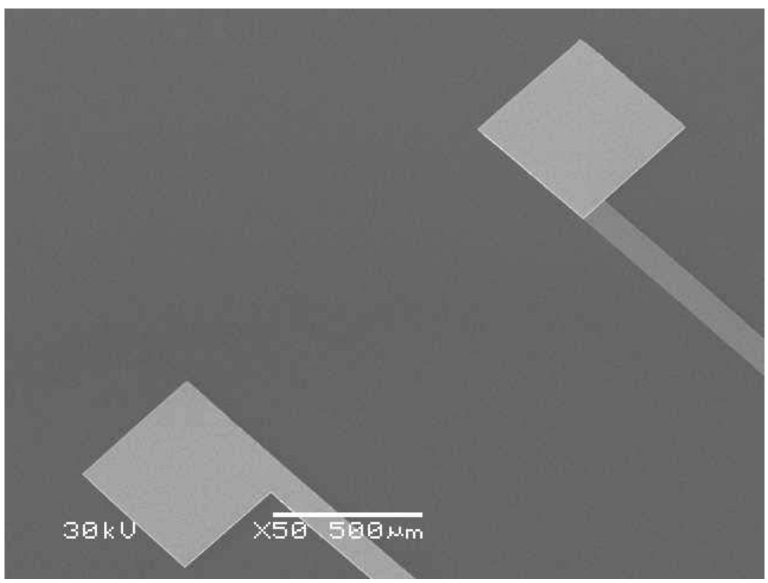


Figure 4: A low-magnification SEM of the ends of the surface electrodes and bond pads of the prototype ET.

Test Setup

All test setup components have been received and are ready for final assembly. We will finish the assembly and start testing the week of 25 January 2010.

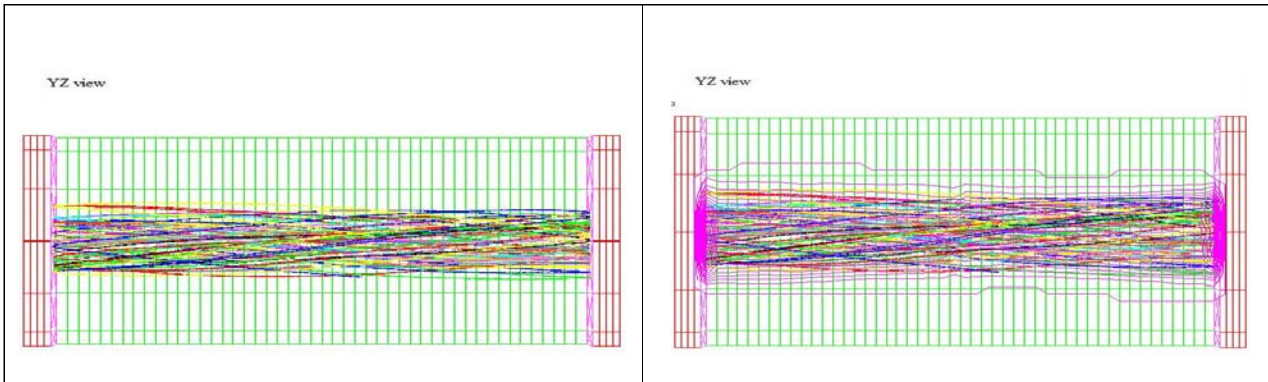
POSITRON TRAPPING AND STORAGE (TASK 2)

Contributors: Washington State University

Deliverable: A representative magnetically based trapping device (not to include the surrounding high flux magnet).

Progress:

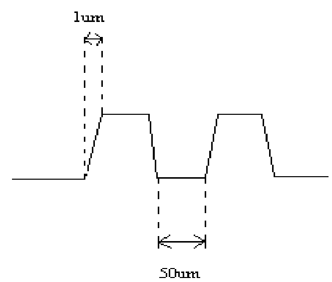
The current program utilized for modeling is the Charged Particle Optics (CPO) program. Several cases have been tested though the CPO program. Currently the trap is built in 3T of magnetic field, and all the cases are set up to investigate the rays with several bounces. We will also test the long-term trap or billion bounces investigation. The tube is about 5.5 mm long and the radius is about 49.5 µm in the middle part and 50.5 µm at the two end caps. We apply 10 V of electrical potentials at the end caps. All the cases presented below are the best results so far, although several issues, including negative kinetic energy, have not been resolved.



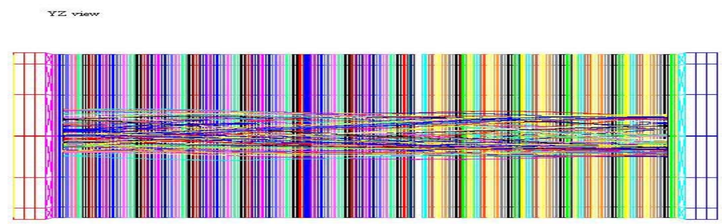
(A)	**(B)**

Figure 5: 20 rays carrying 10 uA are trapped in the tube. Red end-caps and magenta electric fields, green tube with grounded potential walls. (a) YZ view of ray trajectories; all rays start at the middle of the tube parallel with each other. (b) Space charge density contours on YZ view (magneta). The space charge density at the two end caps is higher than in the middle due to the lower velocity of the particles.

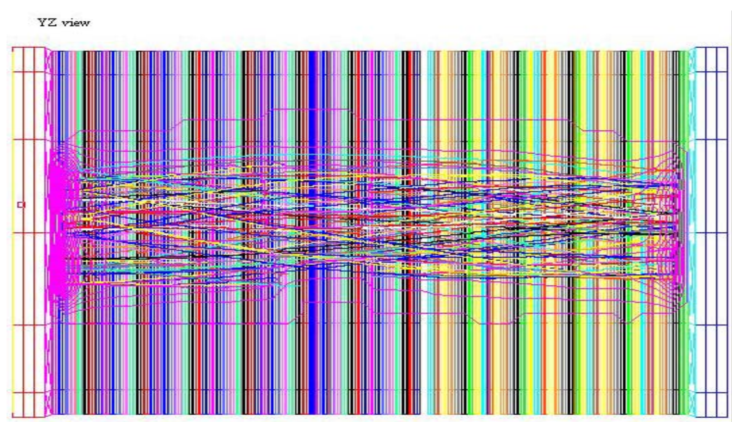
Patch effects on the tube walls are simulated by a varying potential (Figure 6a). Simulation results are shown in Figures 6b and 6c.



(A)



(B)



(C)

Figure 6: Figures from the cases with varying surface potentials on the wall. (a) The potential distribution on the walls of the middle tube. The applied potentials are 0.05 V and 0 V, respectively. (b) The ray trajectories on YZ view. Little difference could be discerned from the one without patch effect (current and other conditions for the ray are the same as the Figure 5).

More work is under way to quantify the “little” differences and to evaluate whether these differences have an effect on the ultimate confinement time of the particles in the trap.

FINANCIAL STATUS

R&D Status Report

Program Financial Status

15 July 2009 through 30 January 2010

Contract Item No.	Current Funding	Current Period Expenses	Cumulative Expenses	% Budget Complete
0001	$1,829,849	$117,417	$576,969	32%
Project Commitments		5,809	263,886	
Total	$1,829,849	$123,226	$840,855	

Based on currently authorized work:

Is current funding sufficient for the current fiscal year (FY)? (Explain if NO) **Yes**

What is the next FY funding requirement at current anticipated levels **N/A (base fully funded)**